BTeV in PHENIX: Pixel Readout Chip Basics

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Names

- **Module** = pixel sensor + readout chips + High Density Interconnect.
- Readout chip = **FPIX2.1** (or maybe FPIX3).
  - **Programming interface** used for initialization and control
  - **Data output interface** used for data output

Initialization & Control

- All I/O is differential LVDS.
- Control is organized by module.
  - Serial bus (4 pairs):
    - BCO Clock,
    - Shift in – input to chip(s),
    - Shift out – output from chip,
    - Shift control – enables chip programming interface.

Command Format

- All commands are formatted as register operations:
  - Command = Chip ID(5 bits) + Register #(5 bits) + Instruction(3 bits) [possibly followed by data].
  - Each chip in a module has an ID (set by wire bonds).
    - 10101 = wild (broadcast command to all chips).
  - Instructions: Write, Set (=1), Reset (=0), Default, Read.

Registers

- Most registers are 8-bit.
- The exceptions are:
  - Kill & Inject are 2816-bit (22x128) consisting of 1 bit in each readout pixel:
    - Kill=1 disables the pixel,
    - Inject=1 connects **Inject In** to the charge injection capacitor associated with the pixel.
  - Active lines (Alines) is a 2-bit register:
    - Sets the number of output pairs to be used for data.
  - SendData and RejectHits are 1-bit registers.
  - Reset commands don’t operate on registers (0-bit).

8-Bit Registers

- Most are used to control bias voltages & currents.
  - Probably won't need to be changed from default values.
- Vth0 – Vth7 set thresholds used by comparators (in 3-bit FADC).
  - Probably will have to be calibrated & set for each readout chip independently.

Data Output Interface

- Master Clock is input to all chips in a module.
- Data output is point-to-point LVDS from each readout chip (not bussed).
- Output clock frequency = Master Clock.
  - Maximum frequency ~ 200 MHz.
  - Does not have to be related to BCO clock, but probably should be for PHENIX.

Data Output – Physical Format

- 1,2,4, or 6 serial links may be used per readout chip.
- An output Data Latch Clock is also sent:
  - ½ MC frequency (rising edges clock odd-number bits, falling edges clock even-number bits in serial output stream).
  - Probably not required (simple digital phase-following in receiver would probably suffice).

More on Data Output

- 24-bit Sync/status word:
  - Used to establish & maintain synchronization with data destination.
  - Is output when chip is idle.
  - Also twice after the “horizontal token” passes column #21.
- 24-bit data word:
  - Row#(7-bits),Column Code(5-bits),BCO#(8-bits),ADC(3-bits),End-of-word mark(1).
- Sync/status word is distinguished by 13 zeros followed by an end-of-word mark(1). The column codes are chosen so that no data word, or sequence of two data words, can contain 13 consecutive zeros.

Readout Sequence

- When a pixel is hit, it associates itself with a **command set** in its End-Of-Column logic that holds the BCO #.
  - The state machine that controls the EOC is clocked by the BCO clock.
  - The next BCO clock moves the command set from listen to idle.
  - Another BCO clock moves the command set from idle to output (something to say).
  - If the chip is idle and any column has something to say, then the horizontal token is launched on the next (internal) **readout clock**.

Readout Sequence (continued)

- All data associated with a single EOC command set is read out.
- The horizontal token is released as readout of the last hit associated with the command set is read out; control passes to the next EOC with something to say.
- When the horizontal token passes column 21, a sync/status word is output while the horizontal token line is reset.
- If any column still has something to say, another sync/status word is output while the horizontal token is launched & reaches the lowest number column with something to say.
- Data is output on each successive (internal) readout clock cycle until the horizontal token again passes column 21.

Time order

- This round-robin readout means that data output by FPIX2.1 chips is not guaranteed to be time-ordered.
- However, I believe that the PHENIX pixel hit rate will be low enough so that essentially all data will be time ordered, even if only 1 serial output line is used per readout chip.

PHENIX DAQ Questions

- Use output DLCLK?
- How many output lines/chip?
- Does data destination need to time-order the data, or can it simply drop data with the “wrong” BCO# before transmitting to the next DAQ level?